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IBM open sources the A2O Core! - Bill Flynn, IBMLive Coding of I2C Core in Verilog, learn FPGAs ~~FPGA Course - RAM Memories #06~~ ~~VERILOG BASED VLSI DESIGN OVERVIEW~~ Verilog with digital blocks in PSoC 5LP **DMA Design Office Tour** Developing application software for Xilinx AXI DMA (Fully Custom IP, Interrupt, and Driver) Embedded Development with Zynq7000 and Zybo Board - Video 3 VIVADO HLS Training AXI Stream interface #07 What is Asynchronous FIFO? || Asynchronous FIFO DESIGN (Clock Domain crossing) Explained in detail. Grand Theft Auto (PC/DOS) 1997, DMA Design, BMG Interactive How to Begin a Simple FPGA Design what is time borrowing (latch) ? why does latches support it?

Synchronous clock vs Asynchronous clock*How I started learning FPGA: My journey writing a GameBoy in Verilog DMA Design logo 1997* ~~KTU CS203 STLD \u0026 CST203 logic circuit design|Module 6 Part 1|Memory and programmable logic~~ *ZYNQ Training - session 03 - axi stream interface* **FFT module on FPGA** Introduction To FIFO Design/FIFO-part 1 Inside Rockstar North (DMA Design)16th May 1996

AXI Memory Mapped Interface \u0026 Hardware Debugging in Vivado (Lesson 5)~~Looking at the PCB \u0026 Chips - Hardware Wallet Research #2~~ ~~Creating Custom AXI Master Interfaces Part 1 (Lesson 7)~~ British Interview with DMA Design in 1996 about Grand Theft Auto ~~Creating Custom AXI Slave Interfaces Part 2 (Lesson 6)~~

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FastVDMA is an open source DMA (Direct Memory Access) controller developed at Antmicro. One of the main motivations leading to the design of an open source DMA controller was the lack of portable open source alternatives to proprietary controllers provided by FPGA vendors. This situation leads to a reduction in the reusability of DMA-based designs into different contexts when adopting multiple kinds of platforms, since DMA solutions tend to be tightly integrated with vendor-specific ...

Antmicro ‧ Antmicro's Fast Versatile DMA: an open ...

Abstract In this paper, the design of Direct Memory Access (DMA) Controller is proposed using Verilog. Direct memory access (DMA) is a feature of modern computers that allows certain hardware...

(PDF) Design and Analysis of DMA Controller for System on ...

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If the state of the design changes after certain duration (see Fig. 7.10), then we need to add the timer in the Verilog design which are created in Listing 7.5 and Listing 7.5. For this, we need to add one more process-block which performs following actions,

7. Finite state machine — FPGA designs with Verilog and ...

Overview. The DMA controller is designed for data transfer in different system environments. Two module types : type 0 and type 1 are provided, and the user can choose the number of each module type. Type 0 modules are designed to transfer data residing on the same bus, and Type 1 modules are designed to transfer data between two different buses. Each module can support up to 4 DMA channels and the IP supports up to 16 total DMA channels.

DMA Controller - Intel

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Basicly the design is the BMD rewritten in vhdl, with working MSI and INTx interrupts, a FIFO backend for the RX and TX engines and a working linux driver for DMA. Able to achive a bandwidth of160 MB/s Tx and 140 MB/s Rx !

DMA reference design in VHDL? - Community Forums

For any questions / remarks / suggestions / bugs please contact info@provartec.com. ----- Opencores.org project - DMA AXI This core is based on the Provartec PR200 IP - 'Generic High performance dual-core AXI DMA' The original IP is a configurable, generic AXI DMA written in RobustVerilog.

GitHub - freecores/dma_axi: AXI DMA 32 / 64 bits

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The FPGA Embedded Design curriculum will take you by the hand through learning Verilog, how to simulate your designs, how to make them real in an FPGA, and finally how to design and use your own Soft Processor. This will take place in a series of courses. This first course is about the Verilog Hardware Description Language.

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As digital circuit elements decrease in physical size, resulting in increasingly complex systems, a basic logic model that can be used in the control and design of a range of semiconductor devices is vital. Finite State Machines (FSM) have numerous advantages; they can be applied to many areas (including motor control, and signal and serial data identification to name a few) and they use less logic than their alternatives, leading to the development of faster digital hardware systems. This clear and logical book presents a range of novel techniques for the rapid and reliable design of digital systems using FSMs, detailing exactly how and where they can be implemented. With a practical approach, it covers synchronous and asynchronous FSMs in the design of both simple and complex systems, and Petri-Net design techniques for sequential/parallel control systems. Chapters on Hardware Description Language cover the widely-used and powerful Verilog HDL in sufficient detail to facilitate the description and verification of FSMs, and FSM based systems, at both the gate and behavioural levels. Throughout, the text incorporates many real-world examples that demonstrate designs such as data acquisition, a memory tester, and passive serial data monitoring and detection, among others. A useful accompanying CD offers working Verilog software tools for the capture and simulation of design solutions. With a linear programmed learning format, this book works as a concise guide for the practising digital designer. This book will also be of importance to senior students and postgraduates of electronic engineering, who require design skills for the embedded systems market.

This book highlights the latest research findings, methods and techniques, as well as challenges and solutions related to Ubiquitous and Pervasive Computing (UPC). In this regard, it employs both theoretical and practical perspectives, and places special emphasis on innovative, mobile and internet services. With the proliferation of wireless technologies and electronic devices, there is a rapidly growing interest in Ubiquitous and Pervasive Computing (UPC). UPC makes it possible to create a human-oriented computing environment in which computer chips are embedded in everyday objects and interact with the physical world. Through UPC, people can remain online even while underway, thus enjoying nearly permanent access to their preferred services. Though it has a great potential to revolutionize our lives, UPC also poses a number of new research challenges.

Uses Verilog HDL to illustrate computer architecture and microprocessor design, allowing readers to readily simulate and adjust the operation of each design, and thus build industrially relevant skills Introduces the computer principles, computer design, and how to use Verilog HDL (Hardware Description Language) to implement the design Provides the skills for designing processor/arithmetic/cpu chips, including the unique application of Verilog HDL material for CPU (central processing unit) implementation Despite the many books on Verilog and computer architecture and microprocessor design, few, if any, use Verilog as a key tool in helping a student to understand these design techniques A companion website includes color figures, Verilog HDL codes, extra test benches not found in the book, and PDFs of the figures and simulation waveforms for instructors

This book concentrates on common classes of hardware architectures and design problems, and focuses on the process of transitioning design requirements into synthesizable HDL code. Using his extensive, wide-ranging experience in computer architecture and hardware design, as well as in his training and consulting work, Ben provides numerous examples of real-life designs illustrated with VHDL and Verilog code. This code is shown in a way that makes it easy for the reader to gain a greater understanding of the languages and how they compare. All code presented in the book is included on the companion CD, along with other information, such as application notes.

Digital Design: An Embedded Systems Approach Using Verilog provides a foundation in digital design for students in computer engineering, electrical engineering and computer science courses. It takes an up-to-date and modern approach of presenting digital logic design as an activity in a larger systems design context. Rather than focus on aspects of digital design that have little relevance in a realistic design context, this book concentrates on modern and evolving knowledge and design skills. Hardware description language (HDL)-based design and verification is emphasized--Verilog examples are used extensively throughout. By treating digital logic as part of embedded systems design, this book provides an understanding of the hardware needed in the analysis and design of systems comprising both hardware and software components. Includes a Web site with links to vendor tools, labs and tutorials. Presents digital logic design as an activity in a larger systems design context Features extensive use of Verilog examples to demonstrate HDL (hardware description language) usage at the abstract behavioural level and register transfer level, as well as for low-level verification and verification environments Includes worked examples throughout to enhance the reader's understanding and retention of the material Companion Web site includes links to tools for FPGA design from Synplicity, Mentor Graphics, and Xilinx, Verilog source code for all the examples in the book, lecture slides, laboratory projects, and solutions to exercises

Verification is increasingly complex, and SystemVerilog is one of the languages that the verification community is turning to. However, no language by itself can guarantee success without proper techniques. Object-oriented programming (OOP), with its focus on managing complexity, is ideally suited to this task. With this handbook—the first to focus on applying OOP to SystemVerilog—we ' ll show how to manage complexity by using layers of abstraction and base classes. By adapting these techniques, you will write more "reasonable" code, and build efficient and reusable verification components. Both a learning tool and a reference, this handbook contains hundreds of real-world code snippets and three professional verification-system examples. You can copy and paste from these examples, which are all based on an open-source, vendor-neutral framework (with code freely available at www.trusster.com). Learn about OOP techniques such as these: Creating classes—code interfaces, factory functions, reuse Connecting classes—pointers, inheritance, channels Using "correct by construction"—strong typing, base classes Packaging it up—singletons, static methods, packages

Verilog HDL is the standard hardware description language for the design of digital systems and VLSI devices. This volume shows designers how to describe pieces of hardware functionally in Verilog using a top-down design approach, which is illustrated with a number of large design examples. The work is organized to present material in a progressive manner, beginning with an introduction to Verilog HDL and ending with a complete example of the modelling and testing of a large subsystem.

Designing a complex ASIC/SoC is similar to learning a new language to start with and ultimately creating a masterpiece using experience, imagination, and creativity. Digital design starts with RTL such as Verilog or VHDL, but it is only the beginning. A complete designer needs to have a good understanding of the Verilog language, digital design techniques, system architecture, IO protocols, and hardware-software interaction. Some of it will come from experience, and some will come with concerted effort. Graduating from college and entering into the world of digital system design becomes an overwhelming task, as not all the information is readily available. In this book, we have made an effort to explain the concepts in a simple way with real-world examples in Verilog. The book is intended for digital and system design engineers with emphasis on design and system architecture. The book is broadly divided into two sections - chapters 1 through 10, focusing on the digital design aspects and chapters 11 through 20, focusing on the system aspects of chip design. This book can be used by students taking digital design and chip design courses in college and availing it as a guide in their professional careers. Chapter 3 focuses on the synthesizable Verilog constructs, with examples on reusable design (parameterized design, functions, and generate structure). Chapter 5 describes the basic concepts in digital design - logic gates, truth table, De Morgan's theorem, set-up and hold time, edge detection, and number system. Chapter 6 goes into details of digital design explaining larger building blocks such as LFSR, scrambler/descramblers, error detection and correction, parity, CRC, Gray encoding/decoding, priority encoders, 8b/10b encoding, data converters, and synchronization techniques. Chapter 7 and 8 bring in advanced concepts in chip design and architecture - clocking and reset strategy, methods to increase throughput and reduce latency, flow-control mechanisms, pipeline operation, out-of-order execution, FIFO design, state machine design, arbitration, bus interfaces, linked list structure, and LRU usage and implementation. Chapter 9 and 10 describe how to build and design ASIC/SoC. It talks about chip micro-architecture, portioning, datapath, control logic design, and other aspects of chip design such as clock tree, reset tree, and EEPROM. It also covers good design practices, things to avoid and adopt, and best practices for high-speed design. The second part of the book is devoted to System architecture, design, and IO protocols. Chapter 11 talks about memory, memory hierarchy, cache, interrupt, types of DMA and DMA operation. There is Verilog RTL for a typical DMA controller design that explains the scatter-gather DMA concept. Chapter12 describes hard drive, solid-state drive, DDR operation, and other parts of a system such as BIOS, OS, drivers, and their interaction with hardware. Chapter 13 describes embedded systems and internal buses such as AHB, AXI used in embedded design. It describes the concept of transparent and non-transparent bridging. Chapter 14 and chapter 15 bring in practical aspects of chip development - testing, DFT, scan, ATPG, and detailed flow of the chip development cycle (Synthesis, Static timing, and ECO). Chapter 16 and chapter 17 are on power saving and power management protocols. Chapter 16 has a detailed description of various power savings techniques (frequency variation, clock gating, and power well isolation). Chapter 17 talks about Power Management protocols such as system S states, CPU C states, and device D states. Chapter 18 explains the architecture behind serial-bus technology, PCS, and PMA layer. It describes clocking architecture and advanced concepts such as elasticity FIFO, channel bonding (deskewing), link aggregation, and lane reversal. Chapter 19 and 20 are devoted to serial bus protocols (PCI Express, Serial ATA, USB, Thunderbolt, and Ethernet) and their operation.

This second edition focuses on the thought process of digital design and implementation in the context of VLSI and system design. It covers the Verilog 2001 and Verilog 2005 RTL design styles, constructs and the optimization at the RTL and synthesis level. The book also covers the logic synthesis, low power, multiple clock domain design concepts and design performance improvement techniques. The book includes 250 design examples/illustrations and 100 exercise questions. This volume can be used as a core or supplementary text in undergraduate courses on logic design and as a text for professional and vocational coursework. In addition, it will be a hands-on professional reference and a self-study aid for hobbyists.